DVB-RCS2 (Digital Video Broadcast - Second Generation DVB Interactive Satellite System) is the latest ETSI standard of the second generation for digital data transmission via satellites. It uses a new 16-state double-binary turbo decoder that significantly outperforms its dated 8-state counterpart of DVB-RCS. DVB-RCS2 is the first standard to adopt these highest performance turbo codes. New modulation schemes (8-PSK and 16-QAM) help to increase spectral efficiency even further. The outstanding error correction performance of the DVB-RCS2 turbo decoder makes it the ideal candidate for further applications where high spectral efficiency is key for lowering costs.

Benefits

- Design-time configuration of throughput for optimal resource utilization.
- Low-power and low-complexity design.
- Burst-to-burst on-the-fly configuration.
- High block length and code rate granularity.
- Configurable amount of turbo decoder iterations for trading-off throughput and error correction performance.
- Legacy DVB-RCS support on request.
- Allows for turbo synchronization to further improve error correction performance.
- Available for ASIC and FPGAs (Xilinx, Altera).

Performance Figures

- Payload throughput of up to 148 Mbit/s at 5 iterations and 92 Mbit/s at 8 iterations (200 MHz).
- BER 10^{-8} with code rate 3/4 at
  - E_S/N_0 = 4.8 dB (QPSK, 298 payload bytes)
  - E_S/N_0 = 8.9 dB (8-PSK, 400 payload bytes)
  - E_S/N_0 = 10.9 dB (16-QAM, 539 payload bytes)

Features

- Compliant with ETSI 301 545-2 V1.1.1 (2012-01) (DVB-RCS2)
- Support for all DVB-RCS2 payload block sizes (14 to 599 bytes) and code rates (1/3 to 7/8)
- Support for all modulation schemes (QPSK, 8-PSK, 16-QAM)

Applications

- Satellite communication
  - Interactive Services
  - Professional Services
- Applications with highest demands on forward error correction
- Applications with the need for a wide range of code rates (1/3 and above) and block lengths

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL or SystemC testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Related Products

DVB-RCS Turbo Decoder

DVB-S2 LDPC/BCH Encoder and Decoder

GEO-Mobile Radio LDPC Decoder

DVB-C2 LDPC/BCH Decoder

802.11n/ac LDPC Decoder

About Creonic

Creonic is an ISO 9001:2008 certified provider of ready-for-use IP cores for several algorithms of communications such as forward error correction (LDPC and Turbo coding), synchronization, and MIMO. The company offers the richest product portfolio in this field, covering standards like DVB-S2X, LTE-A, DVB-RCS2, DOCSIS 3.1, CCSDS, WiFi, WiGig, and UWB. The products are applicable for ASIC and FPGA technology and comply with the highest requirements with respect to quality and performance. For more information, please visit www.creonic.com.

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